Buoyancy-Driven Two Phase Flow and Boiling Heat Transfer in Narrow Vertical Channels

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ABSTRACT

In order to accommodate anticipated 500–1000 kW/m^2 heat fluxes of microelectronic devices with passive immersion cooling, significant enhancement of the pool boiling critical heat flux (CHF) limit of candidate dielectric liquids is required. However, emerging 3-D packaging technologies may present the greatest near-term thermal management challenges. In response, the present study seeks to elucidate the effects of confinement on buoyancy-driven two phase flow and boiling heat transfer to assist in the systematic exploitation of device geometry and extended surfaces for enhanced liquid cooling of 2- and 3-D microelectronic devices.

Microelectronics-scale parallel plate channel boiling experiments were conducted for 20 mm long silicon and aluminum heaters. Channel spacing was varied to provide channel aspect ratios as high as 67, for symmetrically and asymmetrically heated channels. Deteriorated CHF performance is observed with decreasing channel spacing. This behavior is accurately predicted by extending a correlation available in the literature. Silicon heater channels show significant low-flux enhancement at Bond numbers less than 1, and an enhancement mechanism based on vapor and nucleation site interaction effects is proposed.

A methodology for the optimization of immersion cooled 3-D stacked dice is developed, and an equation relating optimum spacing to die length, thickness, and fluid properties is derived. Optimum geometries are found to be able to dissipate hundreds of megawatts per cubic meter. Parametric effects are explored, and modifications to the governing

volumetric heat dissipation optimization equation to address localized device hot spots and other unique phenomena are also addressed.

Finally, a numerical methodology is developed to efficiently explore parametric effects on longitudinal, rectangular plate fin heat sink boiling performance—including, perhaps for the first time, the explicit dependence of fin spacing on boiling heat transfer and CHF. Silicon heat sink performance is observed to continually improve down to the smallest fin spacing investigated, to nearly five times the CHF limit of the unfinned surface. The higher temperature superheats of the polished silicon surfaces and confinement-driven low flux enhancement yield greatly increased heat dissipation. Device heat fluxes of 1000 kW/m^2 may be dissipated by employing higher conductivity heat sink materials or more complex geometries.

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